

## DEVICE PARAMETERS 1/

JPL PART #	MFN	GENERIC PART NO.	RADIATION LEVEL (TID) (RAD(S)) 2/	PACKAGE STYLE	TERMINAL CONNECTIONS	ELECTRICAL PERFORMANCE CHARACTERISTICS	ELECTRICAL TEST REQUIREMENTS	BURN-IN CONNECTION TABLE
12171 - E01060FR	HONEYWELL SSEC	HR1060 - PDA	100K	FIG. 6-3 HEREIN (256-LEAD FLATPACK)	FIG. 6-1 HEREIN	TABLE 5-4 & 5-5 HEREIN	TABLE 5-1 HEREIN	TABLE 5-7 HEREIN

NOTES: 1/ THIS DRAWING, IN CONJUNCTION WITH CS515837B AND MIL-I-38535, LEVEL V, IMPOSES ALL REQUIREMENTS FOR PROCUREMENT OF THESE DEVICES.  
 2/ THE POST-IRRADIATION PARAMETRIC LIMITS SHALL BE THOSE OF TABLES 5-4 & 5-5 HEREIN.  
 3/ THIS STANDARD TAKES PRECEDENCE OVER DOCUMENTS REFERENCED HEREIN.

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	ST 12171	
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## **Scope**

This is the detailed specification for a space-qualified Power Distribution Assembly gate array for the Power Pyro Subsystem. This document shall be the sole source of design specifications for the PDA gate array, and shall supersede any other specification documents issued prior to this release.

## **Applicable Documents**

- o *General Specification for Gate Array Application Specific Integrated Circuits (ASICs), 24 March 1992, CS515837, Rev. B*

This document establishes the general design system, manufacturing and testing requirements for the gate array Application Specific Integrated Circuit (ASIC) parts.

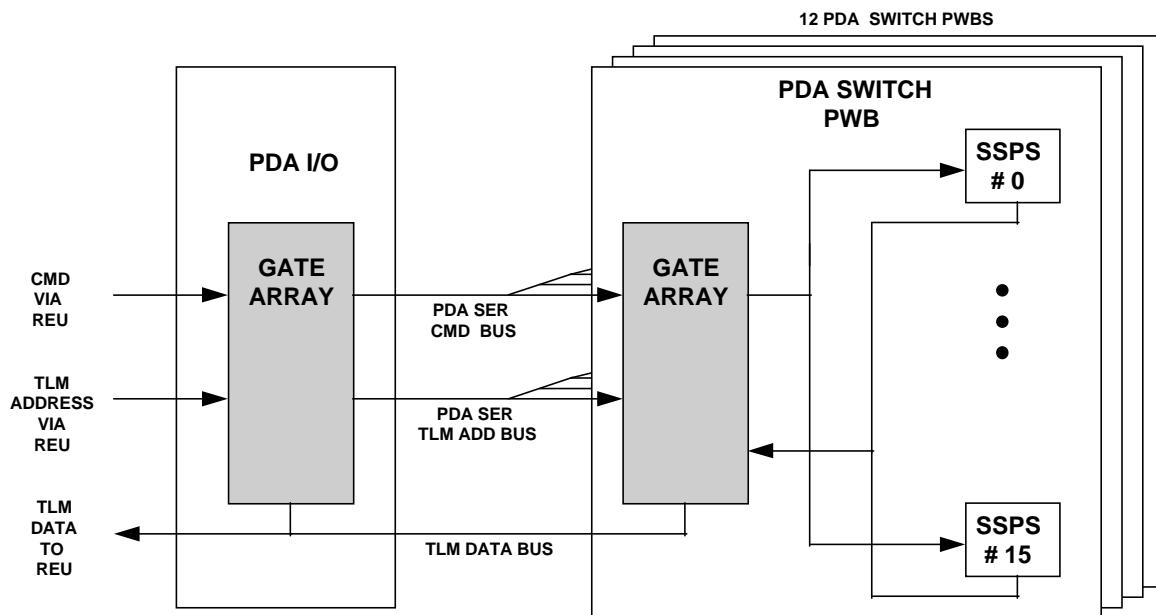
- o *PDA Gate Array Functional Design Criteria. Rev.F, April 2, 1992*

This document provides the functional requirements for the PDA Gate Array design. The information contained in the Performance Criteria section will be used to produce the functional test vectors.

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## 1. CHIP OVERVIEW

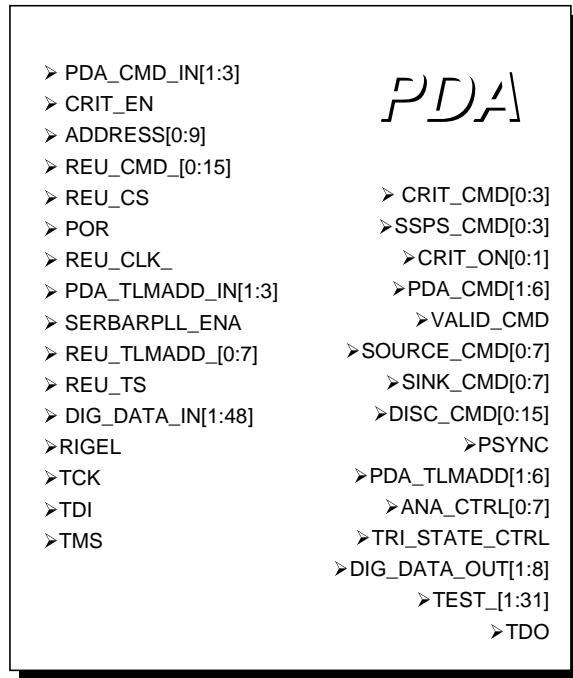
The primary function of the Power Distribution Assembly (PDA) Gate Array is to provide the digital interface for the Solid State Power Switch (SSPS). Each SSPS must be commanded by a Remote Engineering Unit (REU) which is the interface to the spacecraft's communication bus. The PDA Gate Array will provide the digital link to the REU (refer to Figure 1-1. PDA Functional Block Diagram).



**Figure 1-1. PDA Functional Block Diagram**

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## 2. PDA ASIC SIGNAL DESIGNATIONS AND DESCRIPTIONS



**Figure 2-1. PDA ASIC Symbol**

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**Table 2-1. Signal Descriptions**

Name	Pin No. <sup>1</sup>	Type <sup>2</sup>	Description
REU_CMD_(0:15)	7, 8, 10-13, 15-18, 20- 23, 25, 26	IN	Inverted 16 bit parallel command word from the REU
REU_CLK_	27	IN	1 MHz system clock from the REU, 50% ± 5% duty cycle
REU_CS	28	IN	1 µsec ± 5 nsec asynchronous command strobe with REU_CMD(0:15) valid during the strobe
POR	31	IN	Power On Reset signal
REU_TLMADD_(0:7)	33, 34, 37-40, 42, 43	IN	Inverted 8 bit parallel telemetry address from the REU
REU_TS	44	IN	1 µsec ± 5 nsec synchronous telemetry strobe with REU_TLMADD(0:15) valid during the strobe
VALID_CMD	47	OUT3	1 µsec strobe for a valid command
ADDRESS(0:9)	49, 50, 52-59	IN	10 bit "hard-wired" address
PDA_CMD(1:6)	69-72, 74, 75	OUT3	16 bit serial command for the PDA
SOURCE_CMD(0:7)	76, 77, 79-82, 84, 85	OUT6	Discrete source commands for the PSU relay matrix
SINK_CMD(0:7)	86, 87, 89-92, 95, 96	OUT6	Discrete sink commands for PSU relay matrix
DISC_CMD(0:15)	97, 98, 101-104, 106- 109, 111-114, 116, 117	OUT6	Discrete commands for the PCA
PSYNC	118	OUT3	200 kHz synchronization signal to the GPPS
PDA_TLMADD(1:6)	119-124	OUT3	8 bit serial telemetry address for the PDA
PDA_CMD_IN(1:3)	134-136	IN	PDA serial command input
CRIT_EN	138	IN	Critical Command Enable
CRIT_CMD(0:3)	139-141, 143	TRI3	Critical SSPS serial command
SSPS_CMD(0:3)	144-146, 148	OUT3	SSPS serial command
CRIT_ON(0:1)	149, 150	OUT6	Discrete critical SSPS "on" command
SERBARPLL_ENA	151	IN	"Hard-wired" Serial/Parallel enable signal
PDA_TLMADD_IN(1:3)	153-155	IN	Serial telemetry address input
ANA_CTRL(0:7)	159-162, 165-168	OUT3	Discrete analog telemetry address
TRI_STATE_CTRL	170	OUT3	Digital telemetry tri-state control signal

<sup>1</sup> The pin numbers of bus signals are in the same sequence as the signals.

<sup>2</sup> For a description of the signal type refer to Table 5-9.

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**Table 2-1. Signal Descriptions (Cont'd)**

Name	Pin No. <sup>3</sup>	Type <sup>4</sup>	Description
DIG_DATA_OUT(1:8)	171-173, 175-178, 180	TRI3	Multiplexed digital telemetry output
DIG_DATA_IN(1:48)	252-244, 242-239, 237-234, 232-229, 226-223, 220-217, 215-212, 210-207, 205-202, 200-197, 186-184	IN	Digital telemetry data input
Rigel <sup>5</sup>	29	INPD	Rigel test command. Forces internal logic to assume functionality compatible with the Rigel test vector generation tool.
TCK <sup>7</sup>	36	INPD	Test Circuitry Clock. When CDU is being tested using scan path logic, this is the clock for test logic.
TDI <sup>7</sup>	35	INPU	Test Data In. Serial data in for scan path test logic.
TMS <sup>7</sup>	32	INPU	Test Mode Select. Commands the CDU chip scan logic mode.
TRSTN <sup>7</sup>	30	INPU	Test Reset. Resets TAP state machine to the Test-logic reset state which then causes reset of instruction. Upon power-up of the chip, the TRSTN signal must be held low (logic 0) to reset the test logic.
TDO <sup>7</sup>	41	TRI3	Test Output Data. Serial bit stream from the internal scan paths.
TEST_(1:31)	73, 78, 83, 88, 93, 94, 99, 100, 105, 110, 115, 137, 142, 147, 152, 156 158, 163, 164, 169, 174, 181-183, 201, 206, 211, 216, 221, 222	OUT3	Test Outputs.
VDD	2, 64, 66, 128, 130, 192, 194, 256	VDD	Vdd Power Pads.
GND	1, 63, 65, 127, 129, 191, 193, 255	VSS	Vss Power Pads.

<sup>3</sup> The pin numbers of bus signals are in the same sequence as the signals.

<sup>4</sup> For a description of the signal type refer to Table 5-9.

<sup>5</sup> These signals are defined for use with the Honeywell On-Chip Monitor (OCM) scan path control block, and the Rigel test vector generator. See Honeywell manuals for precise definitions of these signals. The OCM is not expected to be used in the flight hardware and therefore it is recommended to tie Rigel, TCK, and TRSTN low (logic 0) and TDI and TMS high (logic 1).

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### 3. FUNCTIONAL DESCRIPTION

The digital link to the REU is divided into two functional designs. The first design, located on the PDA I/O subassembly, is the interface with the REU. This design will process all commands and requests for data from the REU.

The second design is the SSPS interface. Each PDA Switch Subassembly contains 32 SSPS's. SSPS commands have been processed and sent in a serial format from the PDA I/O. These commands are converted to the SSPS format. Data from the 32 SSPS's is multiplexed and sent to the PDA I/O.

Each design is relatively small compared to the capability of the Honeywell HR1060 Gate Array. The two designs can be broken down to the following functional blocks:

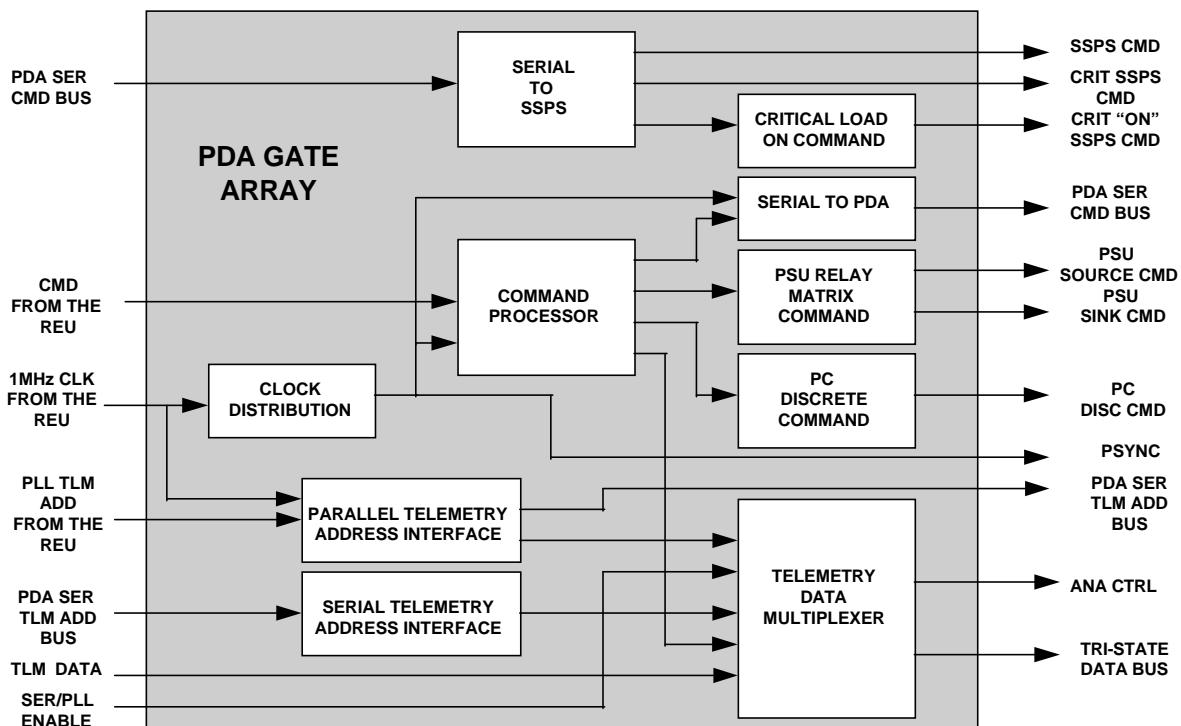


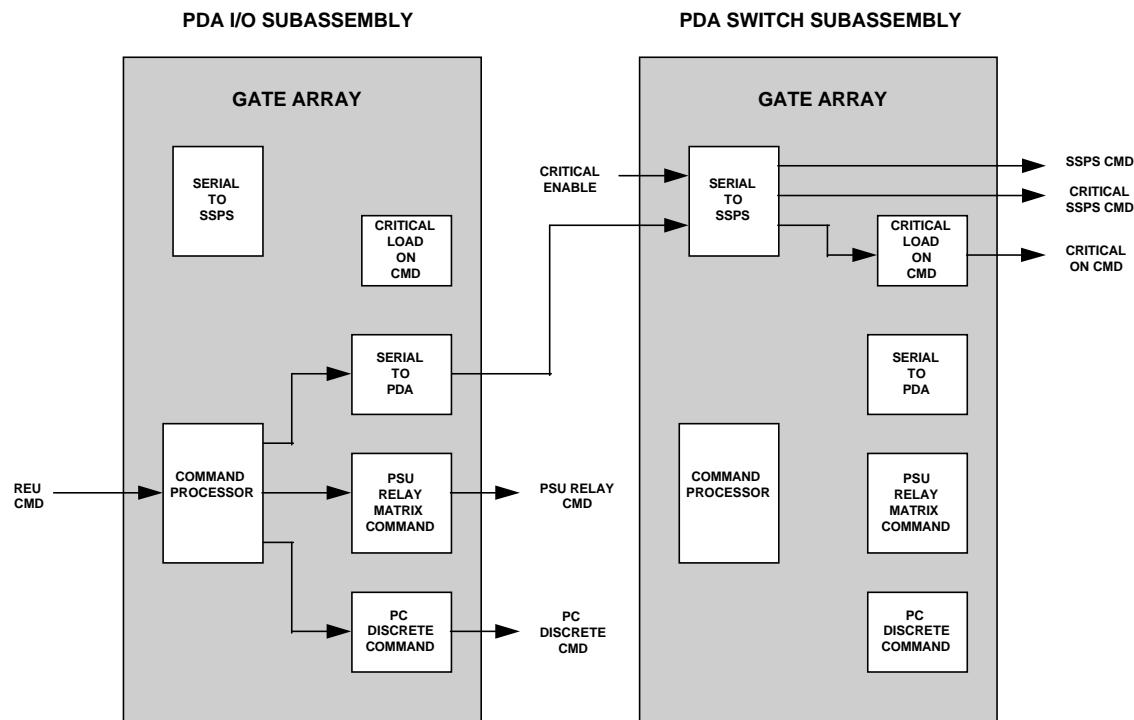
Figure 3-1. PDA Gate Array Functional Block Diagram

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Functional Block	Functional Description
COMMAND PROCESSOR	Process Commands from the REU
SERIAL TO PDA	Provide serial command to PDA Switch Subassembly
PSU RELAY MATRIX COMMAND	Provide discrete PSU relay matrix commands
PC DISCRETE COMMAND	Provide discrete PC relay commands
CLOCK DISTRIBUTION	Provide clocks throughout the system
SERIAL TO SSPS	Provide serial cmd to the SSPS
CRITICAL LOAD ON CMD	Provide discrete "on" command to a critical load SSPS
PARALLEL TELEMETRY ADDRESS INTERFACE	Receive Telemetry address from the REU
SERIAL TELEMETRY ADDRESS INTERFACE	Receive serial address from PDA I/O
TELEMETRY DATA MULTIPLEXER	Multiplex telemetry data

**Table 3-1. PDA Gate Array Functional Blocks**

The gate array can be divided into a command interface and a telemetry interface. The interaction of the two functional designs for the command interface is displayed in figure 3-2: Command Path Functional Block Diagram and for the telemetry interface is displayed in figure 3-3: Telemetry Path Functional Block Diagram.



**Figure 3-2. Command Path Functional Block Diagram**

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CMD[15..0] BITS	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PDA/SSPS	0		BOARD ADD.			SSPS ADD.		*		REU ADD.		P				
PSU	1	1	0		SINK		SOURCE	X		REU ADD.		P				
PC	1	0	0	X	X		DISCRETE		X	REU ADD.		P				
RESET	1	0	1	X	X	X	X	X	X	REU ADD.		P				

\* - ON/OFF  
P - PARITY  
X - DON'T CARE

Table 3-2. PDA Command Table

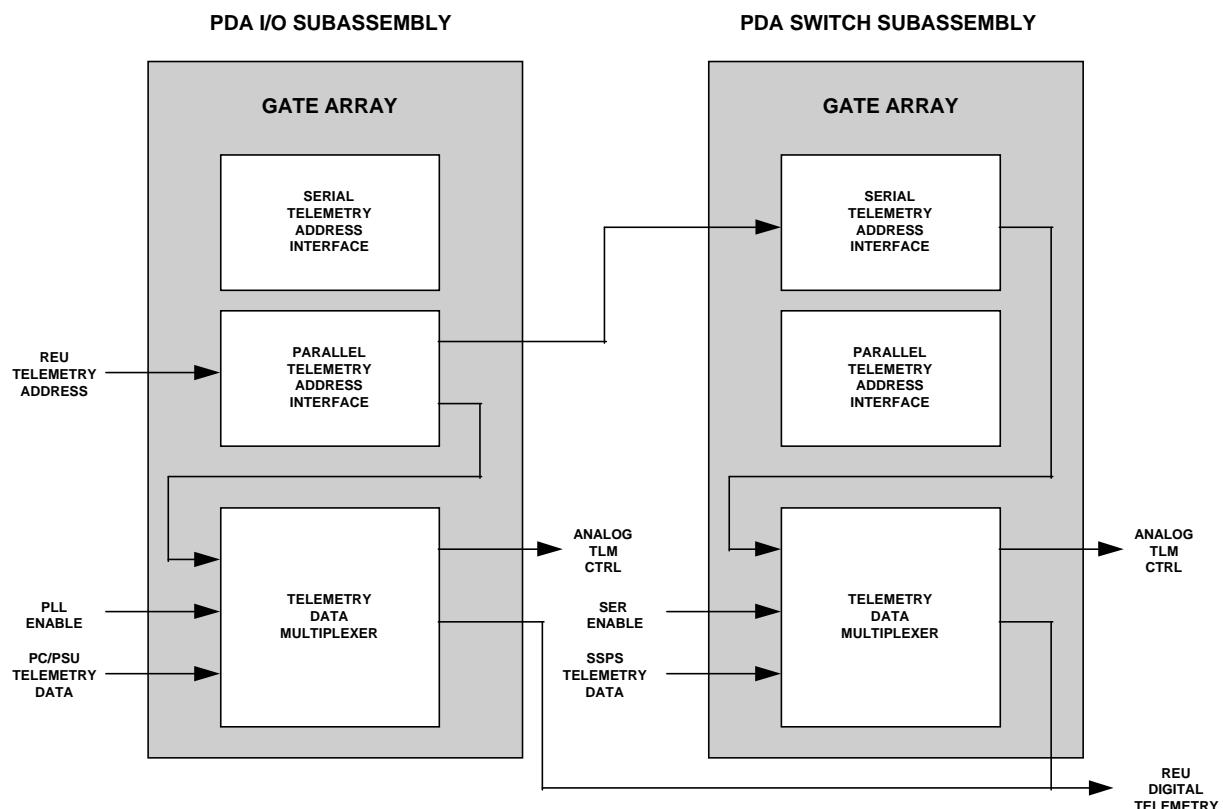


Figure 3-3. Telemetry Path Functional Block Diagram

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ADDRESS BITS	7	6	5	4	3	2	1	0
SSPS DATA ADDRESS	0	X		PDA BOARD ADDRESS		DATA SELECT 1 OF 8		
PC/PSU DATA ADDRESS	1	X		PDA I/O ADDRESS		DATA SELECT 1 OF 8		

X - DON'T CARE

**Table 3-3. PDA Telemetry Address Table**

### 3.1 Command Interface Functional Description

The command interface will process the parallel commands from the REU. Pyro Switching Unit (PSU) and Power Control (PC) commands are converted to discrete commands for relay drivers. SSPS commands are converted to a PDA serial format and driven to all of the PDA Switch Subassemblies. The PDA serial format is converted to the SSPS format on the individual subassemblies. The SSPS serial command fans out to 16 SSPS's.

#### 3.1.1 Command Processor Functional Block

The COMMAND PROCESSOR is the heart of the COMMAND INTERFACE. The processor tests all incoming commands for parity and REU address and maintains a separate count of all passed and failed commands. The processor routes the command to the appropriate address for either the PDA, PSU, or PC.

#### 3.1.2 Serial to PDA Functional Block

The SERIAL TO PDA functional block converts a parallel command from the COMMAND PROCESSOR block to a PDA format serial command. The PDA format contains three signals which provide the serial data, clock and command enable. The inverted form of the three signals is provided for the differential line driver outside of the gate-array.

#### 3.1.3 PSU Relay Matrix Command Functional Block

The PSU RELAY MATRIX COMMAND block provides discrete commands for a matrix of relays. The relay matrix (8 x 8) requires 8 source commands and 8 sink commands. These commands are required to be held for a minimum of 30 msec.

#### 3.1.4 PC Discrete Command Functional Block

The PC DISCRETE COMMAND block provides discrete commands for relay drivers in the PC. These commands are required to be held for a minimum of 15 msec.

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### **3.1.5 Clock Distribution Functional Block**

The CLOCK DISTRIBUTION block distributes the system clock (1 MHz) provided by the REU. The system clock is divided down to 200 KHz for a PSYNC signal.

### **3.1.6 Serial to SSPS Functional Block**

The SERIAL TO SSPS functional block converts the PDA format serial command to the SSPS format serial command. The block provides critical SSPS commands which require an external critical enable. The block converts the serial input to a parallel command bus to be used for the critical on commands in the CRITICAL ON COMMANDS functional block.

### **3.1.7 Critical Load On Command Functional Block**

The CRITICAL LOAD ON COMMAND functional block checks the parallel command from the SERIAL TO SSPS block for parity and board address. A discrete command is produced for an "on" command addressed to the one of the two critical load SSPS's on each circuit board.

## **3.2 Telemetry Interface Functional Description**

The telemetry interface will process all digital data entering the gate array. The REU interface functional design receives a parallel address from the REU requesting data. Multiplexed data from the PSU and the PC is provided to the REU. The SSPS interface design receives a serial address converted by the REU interface. SSPS data is multiplexed for the REU on a tri-state bus connecting all of the PDA Subassemblies together.

### **3.2.1 Parallel Telemetry Address Interface Functional Block**

The PARALLEL TELEMETRY ADDRESS INTERFACE block receives a 8 bit parallel address from the REU. The interface provides the parallel address to the internal multiplexer. The same address is converted to a serial format for the PDA Switch Subassemblies.

### **3.2.2 Serial Telemetry Address Interface Functional Block**

The SERIAL TELEMETRY ADDRESS INTERFACE block receives a serial address and converts it to an 8 bit parallel address. The converted address is provided to the internal multiplexer.

### **3.2.3 Telemetry Data Multiplexer Functional Block**

The TELEMETRY DATA MULTIPLEXER block is a 64 to 8 mux controlled by an 8 bit address. The mux can be hard wired to select the address from either the output of the parallel interface or the serial interface. The mux provides a tri-state output. The block provides decoded control lines for an external analog mux.

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## 4. PERFORMANCE CRITERIA

The performance criteria of the PDA Gate Array is provided for each functional block presented in the previous section (3.). The criteria is broken up into input criteria, output criteria, and timing relationship criteria. The signal name is provided in capital letters.

### 4.1 Command Interface Performance Criteria

#### 4.1.1 Command Processor Functional Block

##### 4.1.1.1 Input Criteria

All inputs to the gate array are driven from 54HCS14 inverters on the same printed wiring board.

REU\_CMD\_[0..15] - 16 bit parallel command generated outside of the gate array to be latched by REU\_CS  
Minimum setup and hold time is 975 nsec and 50 nsec respectively

ADDRESS[5..9] - 5 bit address hard wired outside of the gate array matching the REU address

CLK - 1 MHz clock from CLOCK DISTRIBUTION

REU\_CS - 1  $\mu$ sec ( $\pm$  5 nsec) asynchronous pulse with a valid REU\_CMD\*[0..15] during the pulse

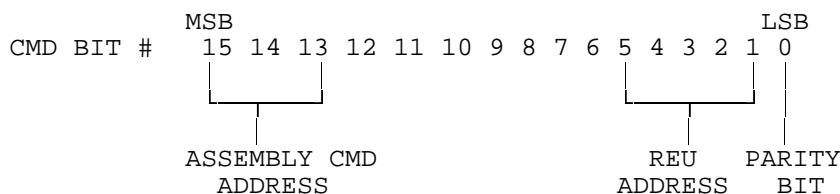
POR - asynchronous power on reset command generated outside the gate array (active low signal)

RIGEL - Rigel test enable active high

##### 4.1.1.2 Output Criteria

All outputs drive internal gate array circuits.

CMD[0..15] - latched inverted REU\_CMD\_[0..15]



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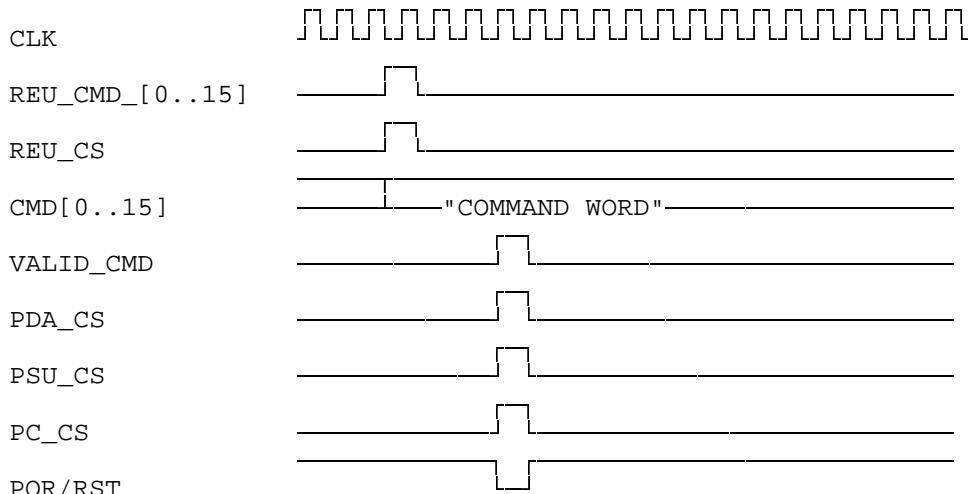
ASSEMBLY CMD ADDRESS	Command Location
0XX	PDA command
110	PSU command
100	PC command
101	Reset command

"X" denotes a "don't care" bit

- VALID\_CMD - 1  $\mu$ sec active high pulse when CMD[0..15] has odd parity and the correct REU address
- CMD\_COUNT[0..7] - eight bits representing a running count on accepted commands
- CMD\_REJECT[0..4] - four bits representing a running count on commands which are rejected due to parity or REU address
- PDA\_CS - 1  $\mu$ sec active high command strobe for PDA commands generated by VALID\_CMD and a correct CMD ADDRESS for the PDA [0XX]
- PSU\_CS - 1  $\mu$ sec active high command strobe for PSU commands generated by VALID\_CMD and a correct CMD ADDRESS for the PSU [110]
- PC\_CS - 1  $\mu$ sec active high command strobe for PC commands generated by VALID\_CMD and a correct CMD ADDRESS for the PC [100]
- POR/RST - can be a 1  $\mu$ sec active low pulse when generated by VALID\_CMD and the correct CMD ADDRESS for command reset [101] or an indefinite length pulse for an externally generated asynchronous power on reset

#### 4.1.1.3 Timing Relationship Criteria

The following timing diagram shows the relationship for all possible command addresses.



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#### **4.1.2 Serial to PDA Functional Block**

##### **4.1.2.1 Input Criteria**

All inputs come from within the gate array.

- |            |  |
|------------|--|
| CMD[0..15] | - 16 bit parallel command provided by the COMMAND PROCESSOR block  |
| PDA_CS     | - 1 $\mu$ sec active high strobe produced in the COMMAND PROCESSOR |
| CLK        | - 1 MHz clock produced from CLOCK DISTRIBUTION                     |
| POR/RST    | - reset command generated in the COMMAND PROCESSOR                 |

##### **4.1.2.2 Output Criteria**

All outputs are the standard 3 mA configurable pads. The outputs drive a CMOS device(54HCS05) on the same printed wiring board.

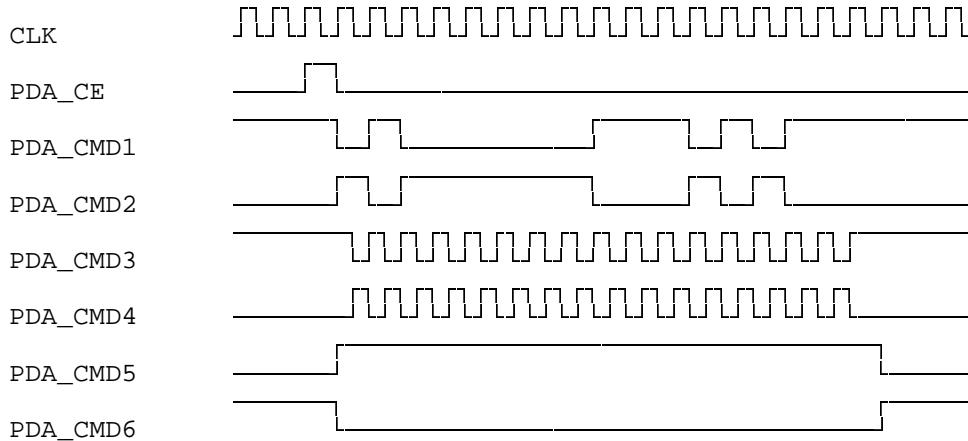
- |          |  |
|----------|--|
| PDA_CMD1 | - 16 bit serial command from CMD[0..15] starting on the rising edge of PDA_CMD5 and is valid on the falling edge of PDA_CMD3 |
| PDA_CMD2 | - inverted PDA_CMD1  |
| PDA_CMD3 | - 16 clocks from CLK   |
| PDA_CMD4 | - inverted PDA_CMD3  |
| PDA_CMD5 | - 17 $\mu$ sec pulse starts with PDA_CMD3  |
| PDA_CMD6 | - inverted PDA_CMD5  |

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#### 4.1.2.3 Timing Relationship Criteria

A command of "0100000011101011" has been sent from the COMMAND PROCESSOR block.

CMD[0..15] - "0100000011101011"

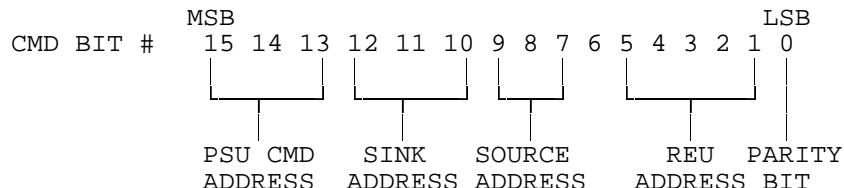


#### 4.1.3 PSU Relay Command Functional Block

##### 4.1.3.1 Input Criteria

All inputs come from within the gate array.

CMD[0..15] - 16 bit parallel command from the COMMAND PROCESSOR



PSU\_CS - 1  $\mu$ sec active high pulse to latch the command word

CLK - 1 MHz clock produced from CLOCK DISTRIBUTION

POR/RST - 1  $\mu$ sec active low command generated in the COMMAND PROCESSOR

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#### 4.1.3.2 Output Criteria

The command length is required to be 30 ms long to hold a non-latching relay closed. Each relay closure requires a source command and a sink command. All outputs are the standard 6 mA configurable pads driving transistor buffers on the same printed wiring board.

SOURCE\_CMD[0..7] - 8 active high discrete commands 40.96 ms in length

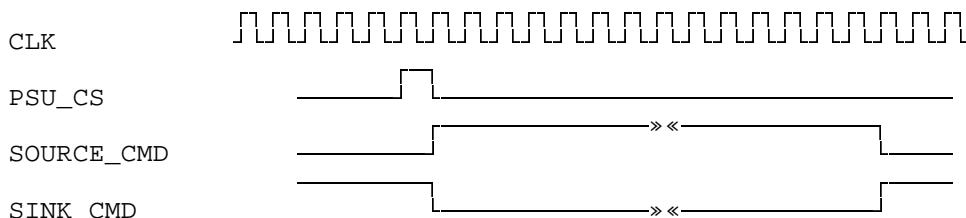
SOURCE_CMD Address	Output
000	SOURCE_CMD0
001	SOURCE_CMD1
010	SOURCE_CMD2
011	SOURCE_CMD3
100	SOURCE_CMD4
101	SOURCE_CMD5
110	SOURCE_CMD6
111	SOURCE_CMD7

SINK\_CMD[0..7] - 8 active low discrete commands 40.96 ms in length

SINK_CMD Address	Output
000	SINK_CMD0
001	SINK_CMD1
010	SINK_CMD2
011	SINK_CMD3
100	SINK_CMD4
101	SINK_CMD5
110	SINK_CMD6
111	SINK_CMD7

#### 4.1.3.3 Timing Relationship Criteria

The following timing diagram shows the relationship between the input and the two selected command outputs within SOURCE\_CMD[0..7] and SINK\_CMD[0..7]. The "»«" denotes an extended 40.96 msec pulse.



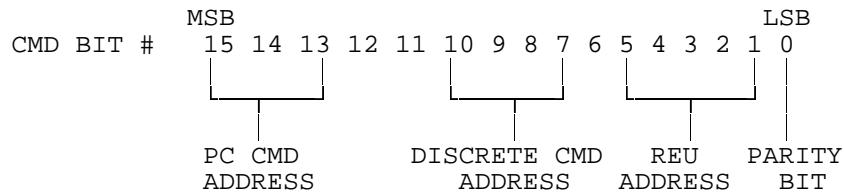
#### 4.1.4 PC Discrete Command Functional Block

##### 4.1.4.1 Input Criteria

All signals come from within the gate array.

CMD[0..15]

- 16 bit parallel command from the COMMAND PROCESSOR



PC\_CS

- 1  $\mu$ sec active high pulse to latch the command word

CLK

- 1 MHz clock produced from CLOCK DISTRIBUTION

POR/RST

- reset command generated in the COMMAND PROCESSOR

##### 4.1.4.2 Output Criteria

All outputs are the standard 6 mA configurable pads driving transistor buffers on the same printed wiring board.

DISC\_CMD[0..15]

- 16 active high discrete commands 40.96 ms in length

DISC_CMD Address	Output
0000	DISC_CMD0
0001	DISC_CMD1
0010	DISC_CMD2
0011	DISC_CMD3
0100	DISC_CMD4
0101	DISC_CMD5
0110	DISC_CMD6
0111	DISC_CMD7
1000	DISC_CMD8
1001	DISC_CMD9
1010	DISC_CMD10
1011	DISC_CMD11
1100	DISC_CMD12
1101	DISC_CMD13
1110	DISC_CMD14
1111	DISC_CMD15

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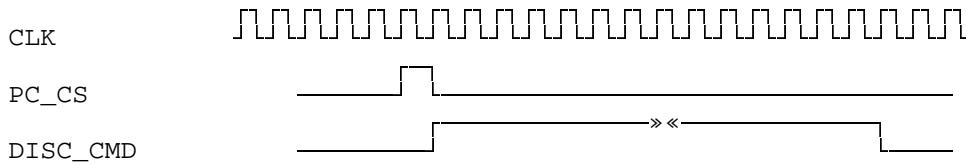
REV. B

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#### 4.1.4.3 Timing Relationship Criteria

The following timing diagram shows the relationship between the input and a selected command output within DISC\_CMD[0..15]. The "»«" denotes an extended 40.96 msec pulse.



#### 4.1.5 Clock Distribution Functional Block

##### 4.1.5.1 Input Criteria

All inputs come from a cmos device (54HCS14) on the same printed wiring board.

REU\_CLK\_ - 1 MHz clock generated outside the gate array ( $50\% \pm 5\%$  duty cycle )

POR/RST - reset command generated from the COMMAND PROCESSOR

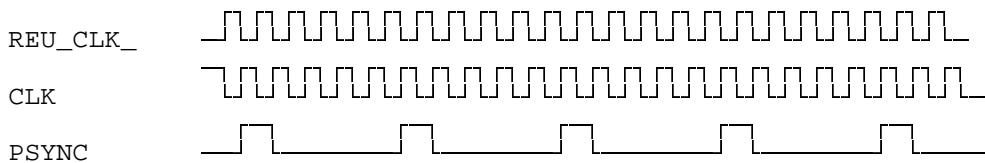
##### 4.1.5.2 Output Criteria

The CLK output is internal to the gate array, however the 200 KHz clock output goes outside to drive a complementary pair of transistors on the same printed wiring board.

CLK - inverted REU\_CLK\_

PSYNC - 200 KHz clock divided down from CLK

##### 4.1.5.3 Timing Relationship Criteria



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#### 4.1.6 Serial to SSPS Functional Block

##### 4.1.6.1 Input Criteria

All inputs come from a CMOS device (54HCS14) on the same printed wiring board.

- |             |  |
|-------------|--|
| PDA_CMD_IN1 | - Serial data which is valid on the falling edge of PDA_CMD_IN2              |
| PDA_CMD_IN2 | - Burst of 16 clocks at 1 MHz which starts on the rising edge of PDA_CMD_IN3 |
| PDA_CMD_IN3 | - 17 $\mu$ sec active high pulse   |
| CRIT_EN     | - CRIT_CMD[0..3] enable signal (active low)                                  |
| POR         | - asynchronous power on reset command (active low)                           |

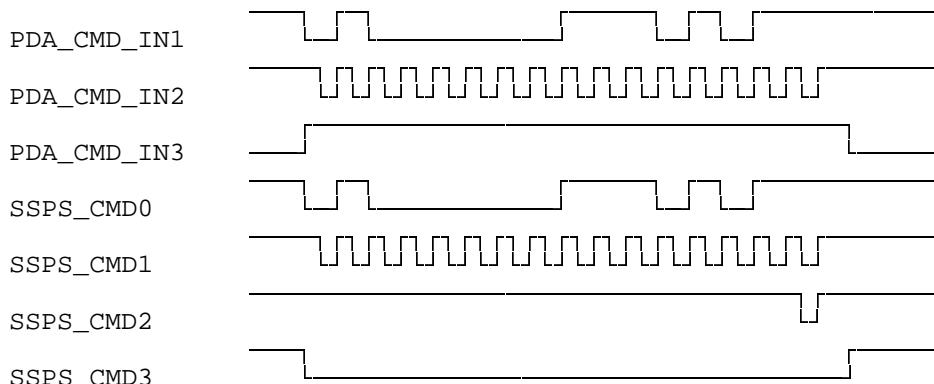
##### 4.1.6.2 Output Criteria

All outputs (except for the internal bus, CRIT\_BUS[0..15]) require 3 mA drivers for a CMOS load(54HCS240).

- |                 |   |
|-----------------|---|
| SSPS_CMD[0..3]  | - Serial command bus containing the following 4 signals.                            |
| SSPS_CMD0       | - same as PDA_CMD_IN1   |
| SSPS_CMD1       | - burst of 16 clocks  |
| SSPS_CMD2       | - 16th clock pulse from PDA_CMD_IN2   |
| SSPS_CMD3       | - inverted PDA_CMD_IN3 (active low)   |
| CRIT_CMD[0..3]  | - Gated SSPS_CMD[0..3] - enabled by a critical enable signal (CRIT_EN - active low) |
| CRIT_BUS[0..15] | - Parallel command converted from PDA_CMD_IN1                                       |

##### 4.1.6.3 Timing Relationship Criteria

A command of "0100000011101011" has been sent to the SERIAL TO SSPS block.



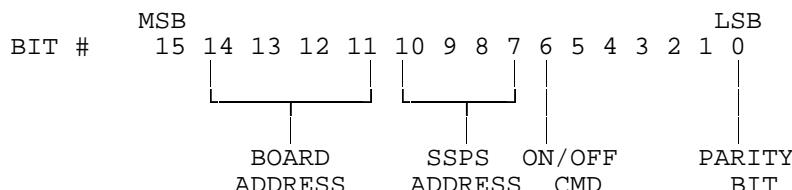
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#### 4.1.7 Critical Load on Command Functional Block

##### 4.1.7.1 Input Criteria

All inputs come from within the gate array except for the hard wired board address.

CRIT\_BUS[0..15] - 16 bit parallel command generated from the SERIAL TO SSPS block



ADDRESS[0..4] - hard wired board address (bit 4 not used)

CS - 500 nsec active low pulse generated in the SERIAL TO SSPS block (same as SSPS\_CMD2)

##### 4.1.7.2 Output Criteria

Each output is the standard 6 mA configurable pad with a 5K pull-up resistor on the output.

CRIT\_ON[0..1] - an active low 500 nsec discrete command generated for an "on" command to SSPS addressed as "0000" or "0001".

##### 4.1.7.3 Timing Relationship Criteria

A command of "0100000011101011" has been provided by the SERIAL TO SSPS functional block.

CRIT\_BUS[0..15] "0100000011101011"



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## 4.2 Telemetry Interface Performance Criteria

### 4.2.1 Parallel Telemetry Address Interface Functional Block

#### 4.2.1.1 Input Criteria

All inputs come from a CMOS device (54HCS14).

REU\_TLMADD\_[0..7] - 8 bit parallel address from the REU to be latched by REU\_TS Minimum setup time is 1.475  $\mu$ sec and the address will be held until the next address 300  $\mu$ sec later

REU\_TS - 1  $\mu$ sec  $\pm$  5 nsec active high telemetry strobe which is high for minimum of 400 nsec before and after the falling edge of REU\_CLK\_

REU\_CLK\_ - 1 MHz system clock used to produce a serial format of the address

POR/RST - reset command generated from the COMMAND PROCESSOR

#### 4.2.1.2 Output Criteria

The complement of the outputs are provided for differential line drivers. Each output requires 3 mA driver for an external CMOS buffer.

PLLTLMADD[0..7] - latched inverted REU\_TLMADD\*[0..7]

PDA\_TLMADD1 - 8 bit serial address valid on the falling edge of PDA\_TLMADD3

PDA\_TLMADD2 - inverted PDA\_TLMADD1

PDA\_TLMADD3 - burst of 8 clock pulses from the system clock

PDA\_TLMADD4 - inverted PDA\_TLMADD3

PDA\_TLMADD5 - active high pulse starting on the first clock in PDA\_TLMADD3 and falling 9 clocks later

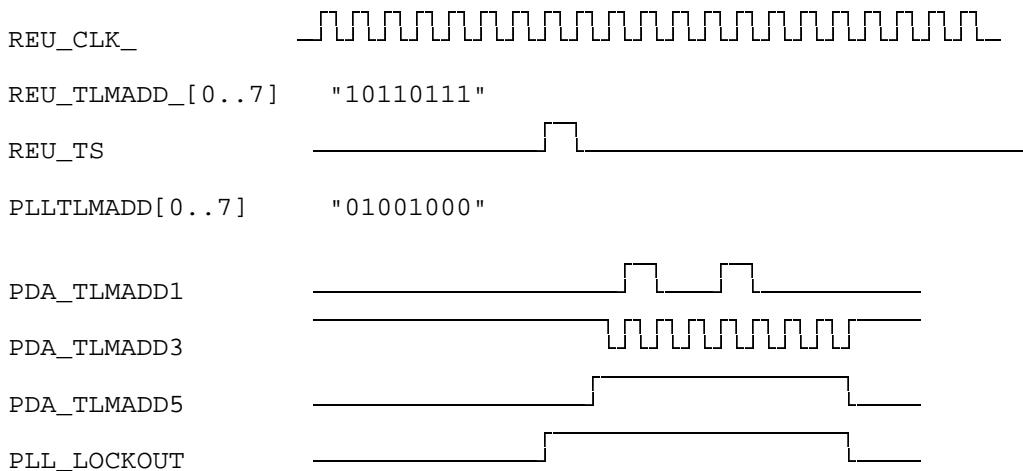
PDA\_TLMADD6 - inverted PDA\_TLMADD5

PLL\_LOCKOUT - 9 1/2  $\mu$ sec active high pulse rising on the rising edge of REU\_TS

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#### 4.2.1.3 Timing Relationship Criteria

The following timing diagram shows an example telemetry address of "01001000".



#### 4.2.2 Serial Telemetry Address Interface Functional Block

##### 4.2.2.1 Input Criteria

All inputs come from a cmos device (54HCS14).

PDA\_TLMADD\_IN1 - 8 bit serial address valid on the falling edge of each clock in PDA\_TLMADD\_IN2

PDA\_TLMADD\_IN2 - burst of 8 clocks

PDA\_TLMADD\_IN3 - active high pulse rising on the first clock and falling a clock after the final clock in PDA\_TLMADD\_IN2

##### 4.2.2.2 Output Criteria

All outputs are contained within the gate array.

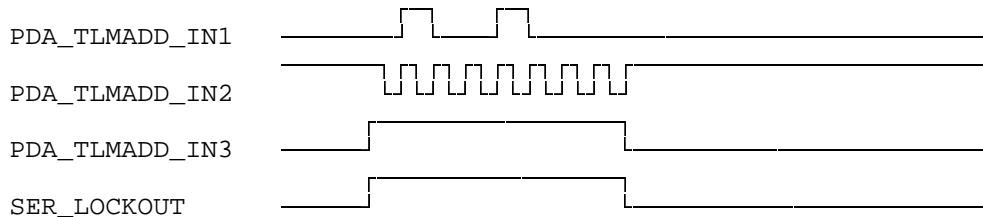
SERTLMADD[0..7] - latched 8 bit parallel address from PDA\_TLMADD\_IN1

SER\_LOCKOUT - 8  $\mu$ sec active high pulse created by PDA\_TLMADD\_IN3

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#### 4.2.2.3 Timing Relationship Criteria

The following timing diagram shows an example telemetry address of "01001000".



#### 4.2.3 Telemetry Data Multiplexer Functional Block

##### 4.2.3.1 Input Criteria

- PLLTLMADD[0..7] - 8 bit parallel address from the PARALLEL TELEMETRY ADDRESS INTERFACE
- SERTLMADD[0..7] - 8 bit parallel address from the SERIAL TELEMETRY ADDRESS INTERFACE
- SERBARPLL\_ENA - hard wired enable
  - low - selects PLL\_TLMADD[0..7]
  - high - selects SER\_TLMADD[0..7]
- ADDRESS[0..4] - external hard wired address for the gate array
- CMD\_REJECT[0..1] - input data from COMMAND PROCESSOR
- CMD\_COUNT[0..7] - input data from COMMAND PROCESSOR
- DIG\_DATA\_IN[1..48] - input data from outside the gate array
- PLL\_LOCKOUT - 9 1/2 µsec active high pulse
- SER\_LOCKOUT - 8 µsec active high pulse

##### 4.2.3.2 Output Criteria

The digital mux outputs are connected to a tri-state bus.

- ANA\_CTRL[0..7] - 8 discrete control lines for analog switches outside the gate array
- TRI-STATE\_CTRL - active low tri-state ctrl line
- DIG\_DATA\_OUT[1..8] - tri-state output of the mux

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## 5. ELECTRICAL CHARACTERISTICS

### 5.1 Electrical Test Requirements

<b>Test</b>	<b>Subgroups</b> (Per MIL-STD-883, Method 5005, Table 1)
Initial (Pre Burn-In)	1,7
Interim (Post Static I Burn-In)	1*,7*
Delta Calculations*,**	
Interim (Post Static II Burn-In)	1*,7*
Delta Calculations*,**	
Final (Post Dynamic Burn-In)	1*,2,3,7*,8,9,10,11
Delta Calculations*,**	
Group A	1,2,3,7,8,9,10,11
Group C End Point electrical***	1,2,3,7,8,9,10,11
Delta Calculations**	

**Table 5-1. Electrical Test Requirements**

- \* PDA applies to these subgroups
- \*\* Deltas shall be calculated relative to the initial electrical parameters. Delta limits of Table 5-8. herein shall apply.
- \*\*\* Group C Lifetest shall be performed using the dynamic burn-in configuration of Table 5-7. herein.

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## 5.2 Absolute Maximum Ratings<sup>6,7,8</sup>

Symbol	Parameter	Ratings		Units
		Min.	Max.	
V <sub>DD</sub>	Supply Voltage	-0.5	7.0	V
V <sub>IN</sub>	Input Voltage Range	GND - 0.5	V <sub>DD</sub> + 0.5	V
I <sub>OUT</sub>	DC Output Current (per Output)		50	mA
P <sub>D</sub>	Max. Package Power Dissipation		4	W
T <sub>ST</sub>	Storage Temperature Range	-65	150	°C
T <sub>S</sub>	Lead Temperature (Soldering, 5s)		270	°C
T <sub>J</sub>	Junction Temperature		175	°C
Θ <sub>JC</sub>	Thermal Resistance, Junction to Case		4	°C/W
V <sub>ESD</sub>	ESD Protection Voltage - Class 2 (MIL-STD-883, Method 3015)	2000		V

**Table 5-2. Absolute Maximum Ratings**

## 5.3 Recommended Operating Conditions<sup>8,9</sup>

Symbol	Parameter	Ratings		Units
		Min.	Max.	
V <sub>DD</sub>	Supply Voltage	4.5	5.5	V
T <sub>A</sub>	Ambient Temperature	-55	125	°C
f <sub>max</sub>	Max. Operating Frequency		1	MHz
t <sub>r</sub> , t <sub>f</sub>	Input Rise Time, Input Fall Time		500	ns

**Table 5-3. Recommended Operating Conditions.**

- 
- <sup>6</sup> Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and effect reliability.
  - <sup>7</sup> Values are guaranteed but not tested.
  - <sup>8</sup> -55°C ≤ T<sub>c</sub> ≤ 125°C except as noted.
  - <sup>9</sup> Extented operation outside recommended limits may degrade performance and effect reliability.

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## 5.4 DC Characteristics

### 5.4.1 DC Electrical Performance Characteristics

Parameter	Symbol	Test Condition	Subgroup	Limit		Unit
				Min	Max	
Input Threshold Voltage	$V_{IH}$	$V_{DD}=5.5V$	1,2,3		3.85	V
	$V_{IL}$	$V_{DD}=4.5V$	1,2,3	1.35		V
Input Leakage Current	$I_{IH1}^{10}$	$V_{DD}=5.5V, V_{IH}=V_{DD}$	1,2,3	-10	10	$\mu A$
	$I_{IH2}^{11}$	$V_{DD}=5.5V, V_{IH}=V_{DD}$	1,2,3	-10	10	$\mu A$
	$I_{IH3}^{12}$	$V_{DD}=5.5V, V_{IH}=V_{DD}$	1,2,3	50	550	$\mu A$
	$I_{IL1}^{10}$	$V_{DD}=5.5V, V_{IH}=GND$	1,2,3	-10	10	$\mu A$
	$I_{IL2}^{11}$	$V_{DD}=5.5V, V_{IH}=GND$	1,2,3	-550	-50	$\mu A$
	$I_{IL3}^{12}$	$V_{DD}=5.5V, V_{IH}=GND$	1,2,3	-10	10	$\mu A$
Output Leakage Current (Tristate)	$I_{OZH}^{13}$	$V_{DD}=5.5V, V_O=VDD$	1,2,3	-10	10	$\mu A$
	$I_{OZL}^{13}$	$V_{DD}=5.5V, V_O=GND$	1,2,3	-10	10	$\mu A$
Output Voltage	$V_{OH1}^{14}$	$V_{DD}=4.5V, I_{OH}=-3mA$	1,2,3	4.0		V
	$V_{OH2}^{15}$	$V_{DD}=4.5V, I_{OH}=-6mA$	1,2,3	4.0		V
	$V_{OL1}^{14}$	$V_{DD}=4.5V, I_{OL}=3mA$	1,2,3		0.5	V
	$V_{OL2}^{15}$	$V_{DD}=4.5V, I_{OL}=6mA$	1,2,3		0.5	V
Output Current	$I_{OH1}^{14}$	$V_{DD}=4.5V, V_{OH}=4.0V$	1,2,3		-3	mA
	$I_{OH2}^{15}$	$V_{DD}=4.5V, V_{OL}=4.0V$	1,2,3		-6	mA
	$I_{OL1}^{14}$	$V_{DD}=4.5V, V_{OH}=0.5V$	1,2,3	3		mA
	$I_{OL2}^{15}$	$V_{DD}=4.5V, V_{OL}=0.5V$	1,2,3	6		mA

Table 5-4. DC Performance Characteristics

<sup>10</sup> All Inputs, except: TDI, TMS, TRSTN, TCK, Rigel

<sup>11</sup> Inputs with Pull-Ups: TDI, TMS, TRSTN

<sup>12</sup> Inputs with Pull-Downs: TCK, Rigel

<sup>13</sup> Tristates and Bidirectionals: TDO, CRIT\_CMD(0:3), DIG\_DATA\_OUT(1:8)

<sup>14</sup> 3mA Outputs: VALID\_CMD, PDA\_CMD(1:6), PSYNC, PDA\_TLMADD(1:6), SSPS\_CMD(0:3), ANA\_CTRL(0:7), TRI\_STATE\_CTRL, CRIT\_CMD(0:3), DIG\_DATA\_OUT(1:8), TDO, TEST\_(1:31)

<sup>15</sup> 6mA Outputs: SOURCE\_CMD(0:7), SINK\_CMD(0:7), DISC\_CMD(0:15), CRIT\_ON(0:1)

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Parameter	Symbol	Test Condition	Subgroup	Limit		Unit
				Min	Max	
Standby Supply Current	I <sub>DDSB</sub>	V <sub>DD</sub> =5.5V, V <sub>IN</sub> =V <sub>DD</sub> or GND, Fc=0 Hz	1,2,3		800	µA
Quiescent Current	I <sub>DDQ</sub>	V <sub>DD</sub> =5.5V, V <sub>IN</sub> =V <sub>DD</sub> or GND, Fc=0 Hz	1		5	µA
Operating Current	I <sub>DDOP</sub> <sup>16</sup>	V <sub>DD</sub> =5.5V, V <sub>IN</sub> =V <sub>DD</sub> or GND, Fc=1 MHz	1,2,3		10	mA
Input Capacitance <sup>17</sup>	C <sub>IN</sub>				15	pF
Output Capacitance <sup>17,18</sup>	C <sub>OUT</sub>				15	pF

**Table 5-4. DC Performance Characteristics (Cont'd)**

#### 5.4.2 Estimated Power Dissipation.

$$P_{\text{Total}} = P_{\text{Internal}} + P_{\text{Outputs}} + P_{\text{Quiescent}} = 3.5 + 8.5 + 4.4 = 16.4 \text{ mW}$$

$$P_{\text{Internal}} = 1/2 * f_{\text{CLK}} * C_{\text{Lint}} * (V_{\text{DD}})^2 = 8.5 \text{ mW}$$

Where:

C <sub>Lint</sub>	=	S * #of Nets * 0.75 pF
S	=	0.25
#of Nets	=	3,000 @ 0.75 pF
f <sub>CLK</sub>	=	1 MHz
V <sub>DD</sub>	=	5.5 V

$$P_{\text{Outputs}} = 1/2 * f_{\text{CLK}} * C_{\text{Lout}} * (V_{\text{DD}})^2 + P_{\text{Crowbar}} = 3.2 + 0.3 = 3.5 \text{ mW}$$

Where:

C <sub>Lout</sub>	=	S * #of Output Pads * 50 pF
S	=	0.04
#of Output Pads	=	104 @ 50 pF
f <sub>CLK</sub>	=	1 MHz
V <sub>DD</sub>	=	5.5 V
P <sub>Crowbar</sub>	=	10% of P <sub>Outputs</sub>

$$P_{\text{Quiescent}} = V_{\text{DD}} * I_{\text{DDSB}} = 4.4 \text{ mW}$$

<sup>16</sup> The operating current is based on the supplied functional test vector set and the ANDO tester loading (85 pF) and may not be applicable to system operation.

<sup>17</sup> Guaranteed but not tested.

<sup>18</sup> Refers to internal capacitance.

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SHEET 31			REV. B	
			SHEET 31	

#### **5.4.3 IDDQ Testing.**

Quiescent Current (IDQ) testing shall be accomplished by using the Stuck-at Fault test vectors generated with RIGEL, or a subset thereof, as determined by JPL. Measurements shall be taken at every vector, unless otherwise indicated, recorded and compared to the IDQ limit. The following statistical values shall be provided: Minimum, Maximum, Mean, Standard Deviation. The IDQ limits shall be established by JPL after characterization of Engineering Model parts which are fabricated from the same wafer lot as the flight parts.

#### **5.4.4 Pulldown Resistors.**

The internal pulldown resistor design option has been used on the following input pads to assure a low state:

TCK  
Rigel

It is recommended that these signals be tied low (logic 0) in the flight hardware.

#### **5.4.5 Pullup Resistors.**

The internal pullup resistor design option has been used on the following input pads to assure a high state:

TDI  
TMS  
TRSTN

It is recommended that the TDI and TMS signals be tied high (logic 1) in the flight hardware. TRSTN must be held low during power-up and therefore is recommended to be tied low (logic 0).

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SHEET 32			SHEET 32	

## 5.5 AC Characteristics

### 5.5.1 AC Electrical Performance Characteristics

Parameter	Symbol	Test Condition $V_{IN}=V_{DD}$ or GND	Subgroup	Specification Limit		Tester Limit <sup>19, 20</sup>		Unit
				Min	Max	Min	Max	
<b>Functional Tests</b>		$V_{DD}=4.5 \text{ & } 5.5V$ $F_c=1 \text{ MHz}$	7,8	pass		pass		
<b>Propagation Delay:</b>		$V_{DD}=4.5 \text{ & } 5.5V$ $F_c=500 \text{ kHz}$						
REU_CLK_↓ to PDA_CMD1	$t_{PLH1}$ $t_{PHL1}$		9,10,11		38		40.0 39.2	ns ns
REU_CLK_↓ to PDA_CMD3	$t_{PLH2}$ $t_{PHL2}$		9,10,11		36		36.0 35.2	ns ns
PDA_CMD_IN2↓ to SSPS_CMD2	$t_{PLH3}$ $t_{PHL3}$		9,10,11		39		36.9 35.8	ns ns
PDA_CMD_IN3↓ to SSPS_CMD3	$t_{PLH4}$ $t_{PHL4}$		9,10,11		28		25.9 24.8	ns ns
<b>Set-up Time:</b>		$V_{DD}=4.5 \text{ & } 5.5V$ $F_c=500 \text{ kHz}$						
PDA_CMD_IN1 to PDA_CMD_IN2↓	$t_{SU1}$		9,10,11	11			11.0	ns
REU_TLMADD_(0:7) to REU_TS↓	$t_{SU2}$		9,10,11	5			5.0	ns
REU_CMD_(0:15) to REU_CS↓	$t_{SU3}$		9,10,11	3			3.0	ns
<b>Hold Time:</b>		$V_{DD}=4.5 \text{ & } 5.5V$ $F_c=500 \text{ kHz}$						
PDA_CMD_IN2↓ to PDA_CMD_IN1	$t_{HD1}$		9,10,11	6			6.0	ns
REU_TS↓ to REU_TLMADD_(0:7)	$t_{HD2}$		9,10,11	16			16.0	ns
REU_CS↓ to REU_CMD_(0:15)	$t_{HD3}$		9,10,11	24			24.0	ns

Table 5-5. AC Performance Characteristics

<sup>19</sup> Tester limits are shown from a test perspective (i.e., set-up time, hold time are shown as max. limits).

<sup>20</sup> Tester limits do not include guardbanding for tester errors.

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SHEET 33			SHEET 33	

## 5.5.2 Timing Analysis.

Pre-layout and post-layout timing shall pass the QuickSim simulation of the vectors supplied to the contractor without setup/hold timing violations.

### 5.5.2.1 Pre-Layout Timing Margins.

Pre-layout timing margins shall be calculated by using standard extreme-value analysis. The extreme values for the cell library shall be supplied by the contractor. Critical paths will be identified and margin calculated via Mentor or Honeywell software toolsets, or a combination thereof.

### 5.5.2.2 Post-Layout Timing Margins.

Post-layout analysis of the device shall show positive margin on internal critical paths over all operating conditions. The analysis will follow the same form as the pre-layout analysis, with the post-layout timing values annotated to the design file by the contractor.

### 5.5.2.3 Tester Specification Limits.

Tester Specification limits in Table 5-5. have been adjusted for modified output levels and for differences in output loading in the ANDO tester environment. Modified output levels are required to account for impedance mismatches between device outputs and the ANDO tester environment. The level at which an output is considered to have switched has been changed from 50% of VDD to 1V for low to high transitions and VDD-0.5V for high to low transitions for the 3mA buffer and to 1V for low to high transitions and VDD-1V for high to low transitions for the higher drive buffers (6mA, 9mA, 12mA, 15mA).

$$t_{\text{SPEC}}(\text{Tester}) = t_{\text{SPEC}}(\text{System}) - (T_{\text{Offset\_fixed}} + C_{\text{Load}} * \text{LoadingFactor})$$

Where:

$$\begin{aligned} C_{\text{Load}} (\text{ System Simulation}) &= 10 \text{ pF} - \text{PDA\_CMD1, PDA\_CMD3} \\ &\quad 20 \text{ pF} - \text{SSPS\_CMD2, SSPS\_CMD3} \end{aligned}$$

For 3 mA drive buffer:

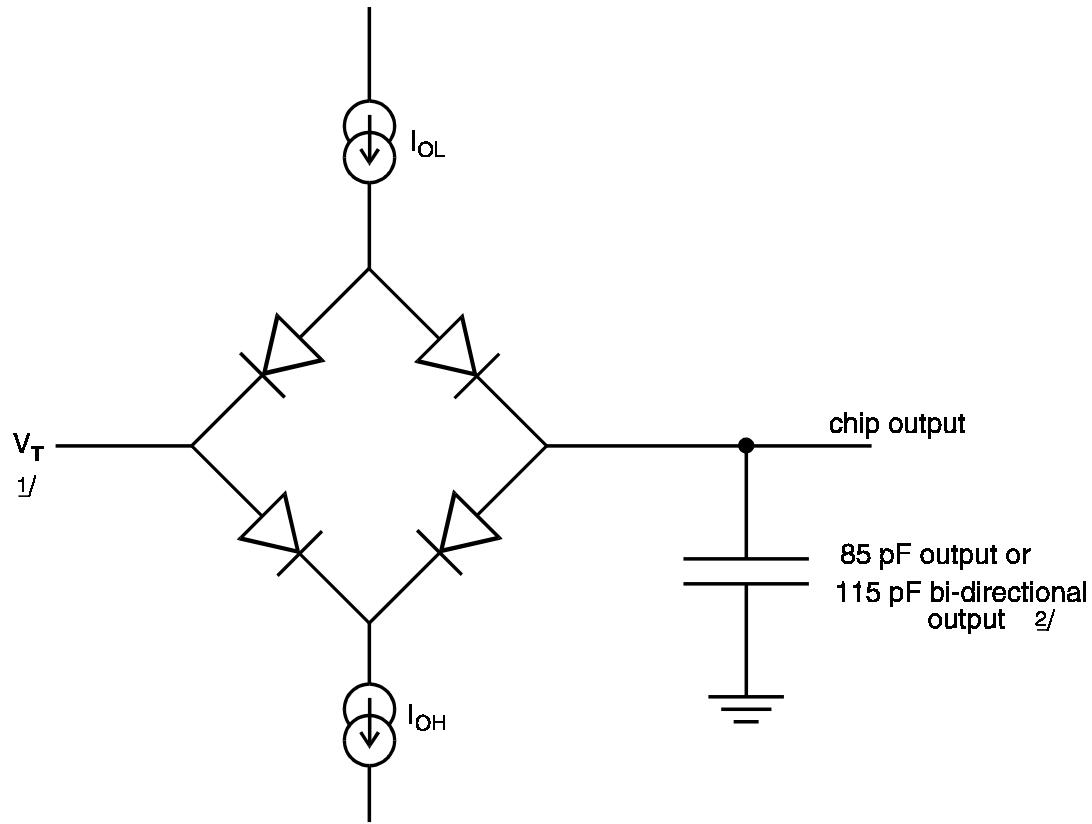
Low to High transition:	$T_{\text{Offset\_fixed}} = -2.0 \text{ ns}$	$\text{LoadingFactor} = 0.205$
High to Low transition:	$T_{\text{Offset\_fixed}} = -1.6 \text{ ns}$	$\text{LoadingFactor} = 0.241$

For 6 mA drive buffer:

Low to High transition:	$T_{\text{Offset\_fixed}} = -1.0 \text{ ns}$	$\text{LoadingFactor} = 0.103$
High to Low transition:	$T_{\text{Offset\_fixed}} = -1.0 \text{ ns}$	$\text{LoadingFactor} = 0.121$

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SHEET 34					

### 5.5.3 Tester Load Circuit



**Figure 5-3. Tester Load Circuit**

- 1/  $V_T$  is a variable dependent upon the test parameter.
- 2/ This capacitance is actually partially distributed through the fixturing so that the device is actually loaded by a transmission line.

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SHEET 35		REV. B SHEET 35	

## 5.6 Burn-In

### 5.6.1 Static Burn-In

The Static Burn-In conditions shall be as specified in JPL General Specification CS 515837, Rev. B. The burn-in configuration shall be as shown in Table 5-7.

### 5.6.2 Dynamic Burn-In

The Dynamic Burn-In conditions shall be as specified in JPL General Specification CS 515837, Rev. B. The burn-in configuration shall be as shown in Table 5-7. Input stimuli (STIM) to exercise the device shall be applied by using the RIGEL Stuck-at Fault test vectors, or a subset thereof, as determined by JPL. At least one output (MON) shall be monitored during burn-in to assure that the output is toggled and the circuit functioning.

### 5.6.3 Burn-In Conditions

	Static I	Static II	Dynamic	QCI - Life Test
Duration	48 hours	48 hours	240 hours	2000 hours
Voltage	6.5 V	6.5 V	6.5 V	6.0 V
+ Tolerance	+0.1V	+0.1V	+0.1V *	+0.1V *
- Tolerance	-0.25V	-0.25V	-0.25V	-0.25V
Temperature	125 °C	125 °C	125 °C	125 °C
+ Tolerance	+5 °C	+5 °C	+5 °C	+5 °C
- Tolerance	-0 °C	-0 °C	-0 °C	-0 °C

**Table 5-6. Burn-In Conditions**

\* Applies to Average Power Supply Voltage. Tolerance for Dynamic Switching Noise is +0.25V.

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SHEET 36		SHEET 36		

#### 5.6.4 Burn-In Configuration

Pin Name	Pin No. <sup>21</sup>	Type <sup>22</sup>	Burn-In Test Connection <sup>23</sup>			Description
			Static I	Static II	Dynamic	
REU_CMD_(0:15)	7, 8, 10-13, 15-18, 20-23, 25, 26	IN	GND	VDD	VDD	Command word
REU_CLK_	27	IN	GND	VDD	VDD	1 MHz system clock
REU_CS	28	IN	GND	VDD	VDD	Command strobe
POR	31	IN	GND	VDD	VDD	Power On Reset
REU_TLMADD_(0:7)	33, 34, 37-40, 42, 43	IN	GND	VDD	VDD	Telemetry address
REU_TS	44	IN	GND	VDD	VDD	Telemetry strobe
VALID_CMD	47	OUT3	GND	VDD	VDD	Strobe for a valid command
ADDRESS(0:9)	49, 50, 52-59	IN	GND	VDD	VDD	"Hard-wired" address
PDA_CMD(1:6)	69-72, 74, 75	OUT3	GND	VDD	VDD	Serial command
SOURCE_CMD(0:7)	76, 77, 79-82, 84, 85	OUT6	GND	VDD	VDD	Discrete source command
SINK_CMD(0:7)	86, 87, 89-92, 95, 96	OUT6	GND	VDD	VDD	Discrete sink command
DISC_CMD(0:15)	97, 98, 101-104, 106-109, 111-114, 116, 117	OUT6	GND	VDD	VDD	Discrete command
PSYNC	118	OUT3	GND	VDD	VDD	Synchronization signal
PDA_TLMADD(1:6)	119-124	OUT3	GND	VDD	VDD	Telemetry address
PDA_CMD_IN(1:3)	134-136	IN	GND	VDD	VDD	Command input
CRIT_EN	138	IN	GND	VDD	VDD	Critical Command Enable
CRIT_CMD(0:3)	139-141, 143	TRI3	GND	VDD	VDD	Critical SSPS serial command
SSPS_CMD(0:3)	144-146, 148	OUT3	GND	VDD	VDD	SSPS serial command
CRIT_ON(0:1)	149, 150	OUT6	GND	VDD	VDD	Discrete critical SSPS "on" command
SERBARPLL_ENA	151	IN	GND	VDD	VDD	Serial/Parallel enable signal
PDA_TLMADD_IN(1:3)	153-155	IN	GND	VDD	VDD	Serial telemetry address
ANA_CTRL(0:7)	159-162, 165-168	OUT3	GND	VDD	VDD	Telemetry address
TRI_STATE_CTRL	170	OUT3	GND	VDD	VDD	Tri-state control signal
DIG_DATA_OUT(1:8)	171-173, 175-178, 180	TRI3	GND	VDD	VDD	Telemetry output
DIG_DATA_IN(1:48)	252-244, 242-239, 237-234, 232-229, 226-223, 220-217, 215-212, 210-207, 205-202, 200-197, 186-184	IN	GND	VDD	VDD	Telemetry data input

Table 5-7. Burn-In Configuration

<sup>21</sup> The pin numbers of bus signals are in the same sequence as the signals.

<sup>22</sup> For a description of the signal type refer to Table 5-9.

<sup>23</sup> All inputs and outputs shall be tied to the specified voltage level through a 2.2 kΩ resistor (±5%, 1/4W).

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SHEET 37			SHEET 37	

Pin Name	Pin No. <sup>24</sup>	Type <sup>25</sup>	Burn-In Test Connection <sup>26</sup>			Description
			Static I	Static II	Dynamic	
Rigel	29	INPD	GND	VDD	STIM <sup>27</sup>	Rigel test command.
TCK	36	INPD	GND	VDD	STIM <sup>27</sup>	Test Circuitry Clock.
TDI	35	INPU	GND	VDD	STIM <sup>27</sup>	Test Data In.
TMS	32	INPU	GND	VDD	STIM <sup>27</sup>	Test Mode Select
TRSTN	30	INPU	GND	VDD	STIM <sup>27</sup>	Test Reset
TDO	41	TRI3	GND	VDD	MON <sup>28</sup>	Test Output Data
TEST_(1:31)	73, 78, 83, 88, 93, 94, 99, 100, 105, 110, 115, 137, 142, 147, 152, 156- 158, 163, 164, 169, 174, 181-183, 201, 206, 211, 216, 221, 222	OUT3	GND	VDD	VDD	Test Outputs
VDD	2, 64, 66, 128, 130, 192, 194, 256	VDD	6.5V	6.5V	6.5V (6V for Lifetest)	Vdd Power Pads.
GND	1, 63, 65, 127, 129, 191, 193, 255	VSS	0.0V	0.0V	0.0V	Vss Power Pads.

**Table 5-7. Burn-In Configuration (Cont'd)**

<sup>24</sup> The pin numbers of bus signals are in the same sequence as the signals.

<sup>25</sup> For a description of the signal type refer to Table 5-9.

<sup>26</sup> All inputs and outputs shall be tied to the specified voltage level through a 2.2 kΩ resistor (±5%, 1/4W).

<sup>27</sup> Stimulated Input

<sup>28</sup> Monitored Output

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SHEET 38					SHEET 38

### 5.6.5 Delta Limits

Symbol	Parameter	Spec. Limits		Units	Delta Limits	Units
		Min	Max			
I <sub>DDSB</sub>	Static Supply Current		800	µA	80	µA
I <sub>IL1</sub>	Input Leakage Current Low: All Inputs except Pull-Ups and Pull-Downs	-10	10	µA	±1	µA
I <sub>IL2</sub>	Input Leakage Current Low: Pull-Ups	-550	-50	µA	±55	µA
I <sub>IL3</sub>	Input Leakage Current Low: Pull-Downs	-10	10	µA	±1	µA
I <sub>IH1</sub>	Input Leakage Current High: All Inputs except Pull-Ups and Pull-Downs	-10	10	µA	±1	µA
I <sub>IH2</sub>	Input Leakage Current High: Pull-Ups	-10	10	µA	±1	µA
I <sub>IH3</sub>	Input Leakage Current High: Pull-Downs	50	550	µA	±55	µA
I <sub>OZL</sub> , I <sub>OZH</sub>	Output Leakage Current	-10	10	µA	±1	µA
I <sub>OL1</sub> , I <sub>OH1</sub>	Output Current: All 3mA Outputs	-3	3	mA	±300	µA
I <sub>OL2</sub> , I <sub>OH2</sub>	Output Current: All 6mA Outputs	-6	6	mA	±600	µA

Table 5-8. Delta Limits

### 5.7 Pin Type Description

Pin Name	Drive	I/O	Type
IN	=	CMOS,	Input Signal
INPU	=	CMOS,	Input Signal with Pull-up
INPD	=	CMOS,	Input Signal with Pull-down
TRI3	= 3mA,	CMOS,	Tri-State Signal
OUT3	= 3mA,	CMOS,	Output Signal
OUT6	= 6mA,	CMOS,	Output Signal

Table 5-9. Pin Type Description

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SHEET 39			REV. B SHEET 39

## 6. PHYSICAL CHARACTERISTICS

### 6.1 Pin Assignment.

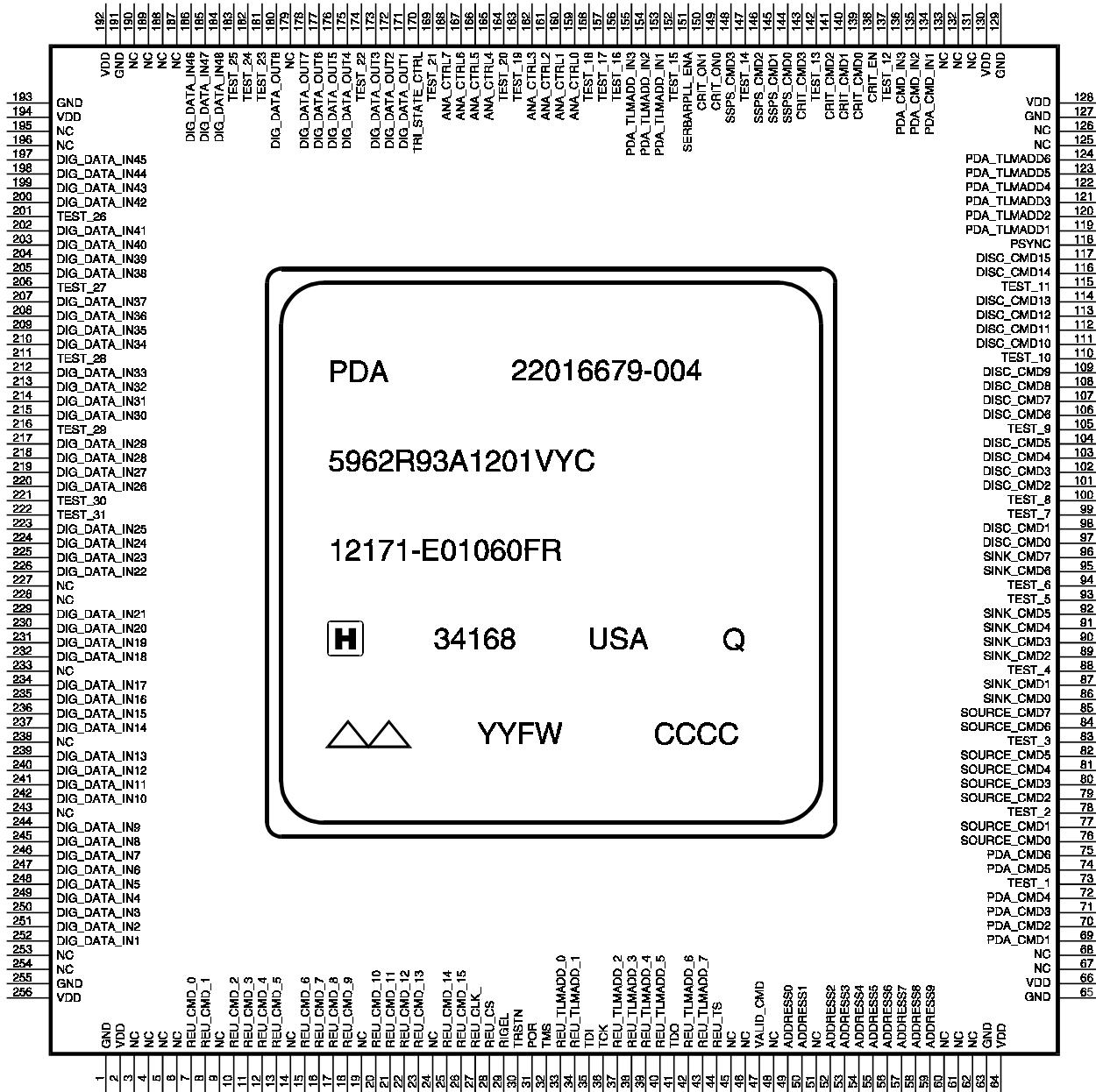
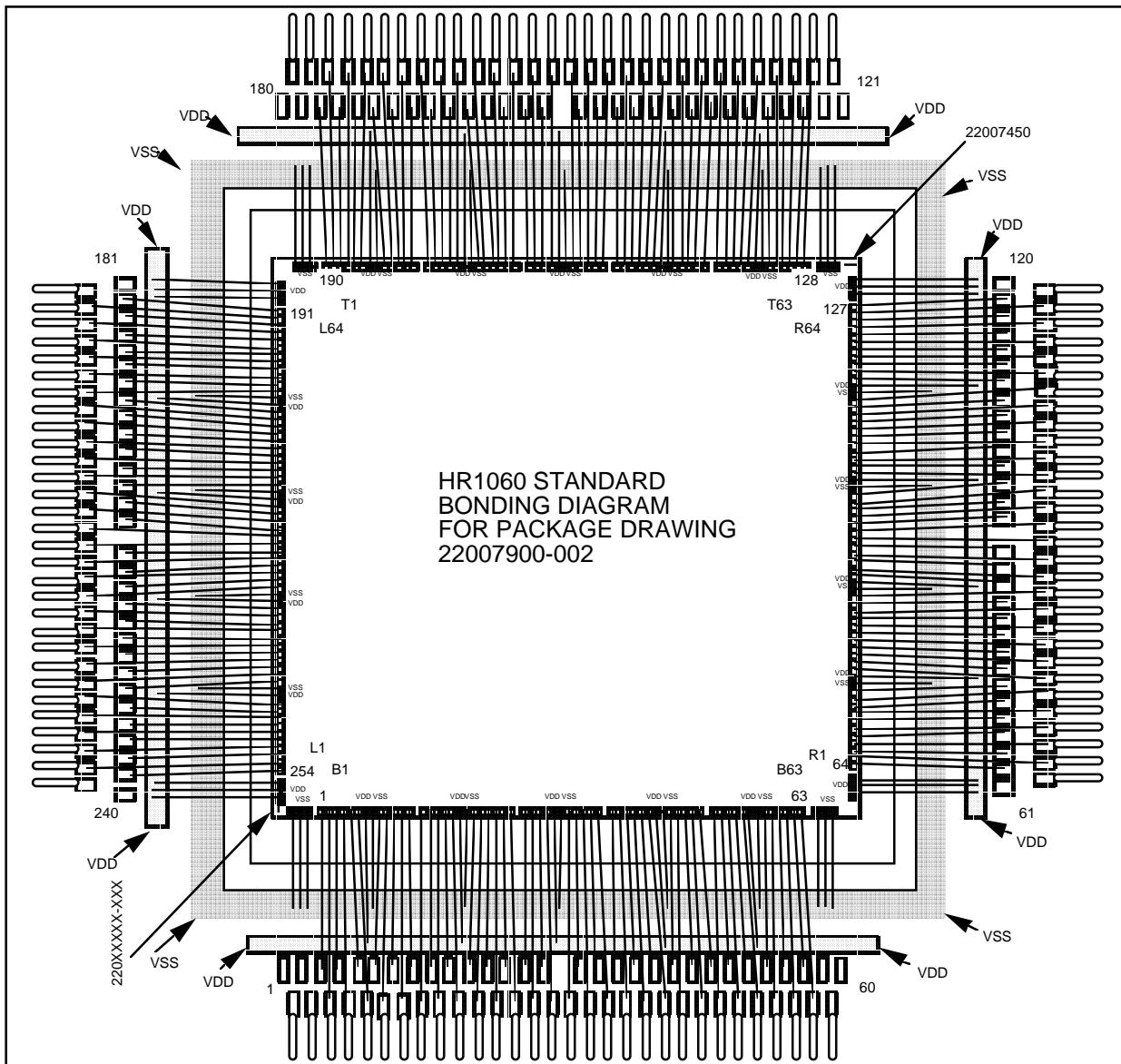


Figure 6-1. PDA ASIC Pinout Assignments

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SHEET 40		REV. B	SHEET 40

## 6.2 Bonding Diagram

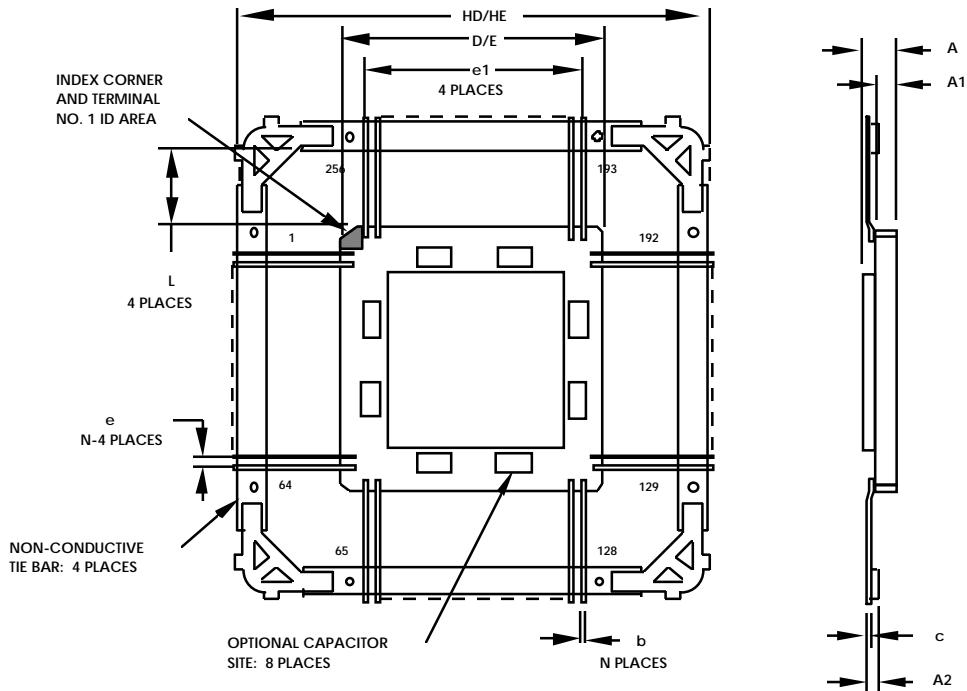


**Figure 6-2. Bonding Diagram (256 pin Flatpack)**

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SHEET 41		REV. B SHEET 41	

### 6.3 Package Outline

#### 256 Lead Flat Package



PACKAGE DIMENSIONS		
Symbol	Dimensions in inches	
	min	max
A	0.130	0.160
A1	-	0.130
A2	0.024	0.040
b	0.005	0.009
c	0.004	0.008
D/E	1.445	1.455
e	0.020 BSC	
e1	1.260 BSC	
HD/HE	2.365	2.395
L	0.325	-
N	256	

Figure 6-3. Package Outline (256 pin Flatpack)

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SHEET 42			SHEET 42	

#### 6.4 Marking Diagram

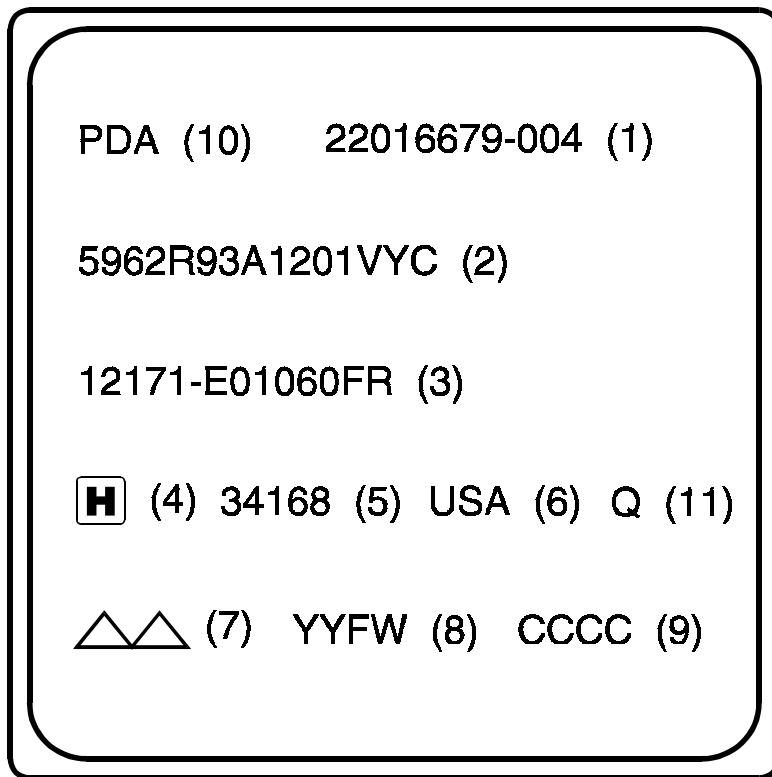


Figure 6-4. Marking Diagram

- (1) Honeywell Part Number
- (2) QML Number (Flight Units only)
- (3) Customer Part Number
- (4) Honeywell Trademark
- (5) Federal Supplier Manufacturing Number
- (6) Country of Origin
- (7) Pin 1 indicator and ESD identifier
- (8) Date Code -Year and Fiscal Week of Lid Seal.  
YY = Year  
FW = Fiscal Week
- (9) Serialization (Traceability Capability to Die)
- (10) Chip Name (If required)
- (11) QML Mark (Flight Units only)

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SHEET 43		REV. B SHEET 43	

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Author: Hubert Schafzahl  
Keywords:  
Comments:  
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Number of Characters: 43,673 (approx.)